PATENT ABSTRACTS OF JAPAN

(11)Publication number : 08-264674

(43)Date of publication of application : 11.10.1996

(51)Int.Cl. H01L 23/04

(21)Application number : 07-060434

(22)Date of filing : 20.03.1995

(71)Applicant : MITSUBISHI ELECTRIC CORP

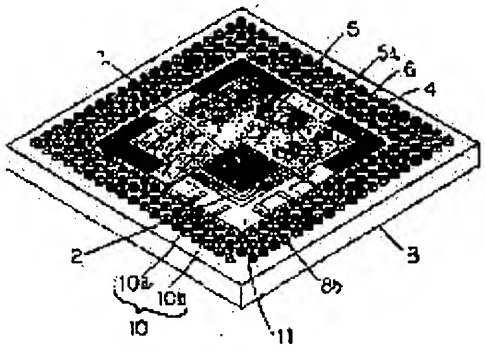
(72)Inventor : UEDA TETSUYA
SHIBATA JUN
YAMA YOMIJI

(54) SEMICONDUCTOR DEVICE

(57)Abstract:

PURPOSE: To maintain a semiconductor device in a thin shape, to make it possible to use a large heat dissipating fin, and to keep a chip part from coming off a substrate by forming lands to mount the chip part at a part opposite a notched plane for a cap.

CONSTITUTION: A notch is formed at a part of a cap 5. And a land 10 for mounting a chip part is formed at a part opposite a notched plane of the hollow cap 5 of a substrate 3. Consequently, when the chip part b is mounted on the land 10, the notch of the cap 5 is facing opposite to this chip part b so that the cap 5 does not extend over the chip part b. Thus, a semiconductor device proper is made into a thin shape. Also, the chip part b is mounted on a cap seal side, making the heat dissipating fin size free from any restriction. Further, since the chip part b is mounted overlapping in the planar directions of the cap 5 and the substrate 3, there is hardly a possibility of its detaching from the substrate due to external environment.



LEGAL STATUS

[Date of request for examination] 09.05.2001

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

* NOTICES *

1. This document has been translated by computer.So the translation may not reflect the original precisely.
2. **** shows the word which can not be translated.
3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]
[Claim 1] The semiconductor device with which a semiconductor chip is carried in the centrum of a substrate, a notch is formed in some aforementioned caps, and the land for chip installation is formed in the portion which counters the flat surface of the notch of the aforementioned cap of the centrum of the aforementioned substrate in the semiconductor device with which the cap seal of this semiconductor chip is carried out, and it changes.
[Claim 2] The semiconductor device with which a semiconductor chip is carried in the centrum of a substrate, and the crevice for chip installation is formed in the portion to which this semiconductor chip does not counter the flat surface of the aforementioned cap of the aforementioned substrate in the semiconductor device which a cap seal is carried out and changes.
[Claim 3] The chip in which the above was attached in the claim 1 or the semiconductor device of 2 is a semiconductor device currently closed with the sealing resin around the aforementioned cap and a cap.
[Claim 4] The semiconductor device with which a semiconductor chip is carried in the centrum of a substrate, and the crevice for chip installation is formed in the portion to which this semiconductor chip counters the flat surface of the aforementioned cap in the centrum of the aforementioned substrate in the semiconductor device which a cap seal is carried out and changes.
[Claim 5] It is the semiconductor device whose aforementioned chip is a chip capacitor in either to claims 1-4.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention relates to the semiconductor device which has the hollow type semiconductor package which carries out the cap seal of the semiconductor chip to the centrum of a multilayer-interconnection substrate.
[0002]
[Description of the Prior Art] The perspective diagram and drawing 10 which show the semiconductor package of the former [drawing 9] are the cross section. The wire which a semiconductor chip and 2 become from aluminum or gold in these drawings in 1, The multilayer-interconnection substrate which 3 becomes from FR4 or BT resin, the solder ball with which 4 consists of lead and tin, The cap which 5 becomes from BT resin or a ceramic, the sealing resin with which 6 closes a cap 5, The metal plate with which 7 consists of copper or a copper alloy, the small capacity chip capacitor which 8a becomes from a ceramic, the mass chip capacitor which 8b becomes from a ceramic, and 9 are radiation fins which consist of aluminum or copper.
[0003] Thus, in the conventional hollow type semiconductor package, two or more solder balls 4 are arranged on the front face on the multilayer-interconnection substrate 3, and the wire 2 which connects a semiconductor chip 1 and a semiconductor chip 1, and the multilayer-interconnection substrate 3 to the centrum of multilayer-interconnection substrate 3 center is contained, and the seal of these semiconductor chips 1, wires 2, etc. is further done by the cap 5. On the other hand, the metal plate 7 which consists of copper or a copper alloy for radiating the heat from a semiconductor chip 1 etc. is formed in the center of a front face of the multilayer-interconnection substrate 3, and the radiation fin 9 which consists of aluminum or copper is further attached on this metal plate 7.
[0004]
[Problem(s) to be Solved by the Invention] By the way, the above chip capacitors 8a and 8b are required in order to achieve an operation of the noise rejection for securing the rapidity of the semiconductor chip exceeding 50MHz etc. And in the conventional semiconductor device, as such chip capacitors 8a and 8b are shown in drawing 10 , mounting in the front face of the aforementioned multilayer-interconnection substrate 3 is performed.
[0005] However, as shown, for example in drawing 10 , when small capacity chip-capacitor 8a is mounted in the front face of the multilayer-interconnection substrate 3, it is necessary to attach a radiation fin 9 on chip-capacitor 8a, and there is a problem that the thickness of the whole semiconductor device will become large. Moreover, as shown in drawing 10 , when mass chip-capacitor 8b is mounted in the front face of the multilayer-interconnection substrate 3, this mass chip-capacitor 8b must be avoided, it is necessary to attach a radiation fin 9, size of a radiation fin 9 must be made so small, and there is a problem that efficient and sufficient discharge of the heat from a semiconductor chip 1 cannot be performed. Furthermore, as shown in drawing 10 , when mass chip-capacitor 8b etc. is mounted in the front face of the multilayer-interconnection substrate 3, there is a problem that a chip capacitor will separate from a substrate 3 by the external environment.

[0006] this invention was made paying attention to the trouble of such conventional technology, even if it mounts chips, such as a chip capacitor, it can maintain the whole semiconductor device at a thin shape, even if it mounts chips, such as a chip capacitor, a radiation fin can use the thing of big size, and it aims at offering a semiconductor device without a possibility that chips, such as a chip capacitor, may separate from a substrate further.
[0007]
[Means for Solving the Problem] In the semiconductor device by this invention for solving such a technical problem, a semiconductor chip is carried in the centrum of a substrate, a notch is formed in some aforementioned caps in the semiconductor device with which the cap seal of this semiconductor chip is carried out, and it changes, and the land for chip installation is formed in the portion which counters the flat surface of the notch of the aforementioned cap of the centrum of the aforementioned substrate.
[0008] Moreover, in the semiconductor device by this invention, a semiconductor chip is carried in the centrum of a substrate and the crevice for chip installation is formed in the portion to which this semiconductor chip does not counter the flat surface of the aforementioned cap of the aforementioned substrate in the semiconductor device which a cap seal is carried out and changes.
[0009] Moreover, as for the chip in which the above was attached in the semiconductor device by this invention, it is desirable to be closed with the sealing resin around the aforementioned cap and a cap.
[0010] Moreover, in the semiconductor device by this invention, a semiconductor chip is carried in the centrum of a substrate and the crevice for chip installation is formed in the portion to which this semiconductor chip counters the flat surface of the aforementioned cap in the centrum of the aforementioned substrate in the semiconductor device which a cap seal is carried out and changes.
[0011] As for the aforementioned chip, in the semiconductor device by this invention, it is still more desirable that it is a chip capacitor.
[0012]
[Function] As mentioned above, in the semiconductor device by this invention, a notch is formed in some aforementioned caps and the land for chip installation is formed in the portion which counters the flat surface of the notch of the aforementioned cap of the centrum of the aforementioned substrate. Therefore, in this invention, when a chip is attached in the aforementioned land, a cap's notch counters on this chip and a cap covers a chip top. That is, in this invention, a chip and a cap are stationed so that it may lap mutually in the direction of a flat surface of a substrate, and so that it may not lap mutually in the thickness direction of a substrate. Therefore, the whole semiconductor device comes to be thin-shape-ized. Moreover, in this invention, since a chip is attached in the cap-seal side of a substrate and does not interfere with the radiation fin by the side of the front face of a substrate, it is lost that the size of a radiation fin is restricted of it by the chip like before. Furthermore, by this invention, since a chip is attached in a position so that it may lap with the aforementioned cap in the direction of a flat surface of a substrate, most possibility of separating from a substrate by the external environment disappears.
[0013] Moreover, the crevice for chip installation is formed in the portion which does not counter the flat surface of the aforementioned cap of the aforementioned substrate in the semiconductor device by this invention. Therefore, in this invention, when a chip is attached in the aforementioned crevice, a cap flat surface does not counter to this chip. That is, in this invention, a chip and a cap are stationed so that it may lap mutually in the direction of a flat surface of a substrate, and so that it may not lap mutually about the thickness direction of a substrate. Therefore, the whole semiconductor device comes to be thin-shape-ized. Moreover, in this invention, since a chip is attached in the cap-seal side of a substrate and does not interfere with the radiation fin by the side of the front face of a substrate, it is lost that the size of a radiation fin is restricted of it by the chip like before. Furthermore, by this invention, since a chip is attached in a position so that it may lap with the aforementioned cap in the direction of a flat surface of a substrate, most possibility of separating from a substrate by the external environment disappears. In addition, in this invention, the crevice for the aforementioned chip installation may be prepared in the centrum of a substrate, and may be prepared out of the centrum of a substrate.
[0014] Moreover, in the semiconductor device by this invention, it can prevent now completely that a

chip separates from the chip in which the above was attached from a substrate by the external environment by closing with the sealing resin around the aforementioned cap and a cap.
[0015] Moreover, the crevice for chip installation is formed in the portion which counters the flat surface of the aforementioned cap of the centrum of the aforementioned substrate in the semiconductor device by this invention. Therefore, in this invention, when a chip is attached in the aforementioned crevice, although this chip becomes the relation which overlap mutually in the thickness direction of a substrate to a cap, since it is attached in the crevice formed in the centrum, it does not become the relation in which it interferes mutually with a cap in the direction of a flat surface of a substrate. Therefore, the whole semiconductor device comes to be thin-shape-ized. Moreover, in this invention, since a chip is attached in the cap-seal side of a substrate and does not interfere with the radiation fin by the side of the front face of a substrate, it is lost that the size of a radiation fin is restricted of it by the chip like before. Furthermore, by this invention, since a chip is attached in a position so that it may lap with the aforementioned cap in the direction of a flat surface of a substrate, most possibility of separating from a substrate by the external environment disappears.
[0016] It is made to attach a chip capacitor as the aforementioned chip in the semiconductor device by this invention furthermore. Therefore, even when attaching the capacitor for noise rejection, in order to attach on the surface of a substrate like before, it is lost that the thickness of the whole semiconductor device becomes large. Moreover, it becomes, without the size of a radiation fin being restricted by the capacitor attached in the substrate front face like before. Furthermore, it comes to be prevented that the capacitor attached in the substrate front face separates by the external environment etc.
[0017]
[Example]
The perspective diagram and drawing 2 which show a semiconductor device [in / the example 1 of this invention / in example 1. drawing 1] are the cross section of the semiconductor device of this example 1. The wire which a semiconductor chip and 2 become from aluminum or gold in these drawings in 1, The multilayer-interconnection substrate which 3 becomes from FR4 or BT resin, the solder ball with which 4 consists of lead and tin, The cap and 5a which 5 becomes from BT resin or a ceramic A cap's height, The cap resin with which, as for a wrap sealing resin and 6a, a cap 5 and a chip capacitor are applied to 6 by a cap's 5 inferior surface of tongue, the metal plate with which 7 consists of copper or a copper alloy, the mass chip capacitor which 8b becomes from a ceramic, and 9 are radiation fins which consist of aluminum or copper. Moreover, in drawing, 10 is the land which consists of conductors, such as gold or copper, and consists of power supply layer 10a inside the multilayer-interconnection substrate 3, and an outgoing line of grand layer 10b. Moreover, in drawing, 11 is the wrap sealing section by the sealing resin 6 about the multilayer-interconnection substrate 3 and a cap 5.
[0018] In addition, in this example, a portion without the aforementioned height 5a in the aforementioned cap's 5 periphery section is equivalent to the "notch" portion of the cap 5 who says this invention. Moreover, the sealing section 11 put into the aforementioned sealing resin 6 has countered this cap's 5 "notch" portion in the thickness direction of a substrate 3. That is, in this example, the aforementioned cap 5 is formed so that there may be no portion of the cap 5 who counters in the substrate thickness direction to the field portion of chip-capacitor 8b, and the portion may serve as a "notch." moreover, the portion which does not counter in the substrate thickness direction to the field portion of a cap's 5 aforementioned chip-capacitor 8b -- above -- a notch -- him -- height 5a is formed in the meaning that there is no **** This height 5a is used in order to position a cap 5 with high precision to the centrum of a substrate 3 when attaching a cap 5, and contacted by the wall side of the centrum of a substrate 3.
[0019] Moreover, in this example, the land 10 which pulled out the conductor from the multilayer-interconnection substrate 3 interior is formed in the sealing section 11 which attaches chip-capacitor 8b. When closing a cap 5 in the sealing section 11, after attaching chip-capacitor 8b in a land 10 by the electroconductive glue (illustration ellipsis), a cap 5 is closed by the cap resin 6, and it is made to cover chip-capacitor 8b by the sealing resin 6 after that. In addition, although a cap 5 is closed by the sealing resin 6, a cap 5 is closed by the cap resin 6 before a wrap and it is made to cover chip-capacitor 8b by

the sealing resin 6 after that in this example 1, without using the cap resin 6, chip-capacitor 8b is attached in a land 10 by the electroconductive glue (illustration ellipsis), and it is good [in a cap 5 and the aforementioned chip-capacitor 8b] by the sealing resin 6 as for a method of a wrap after that.
[0020] As mentioned above, according to this example, since two or more mass chip-capacitor 8b is prepared in the cap 5 side of a substrate 3, for example, it can fully secure also by the rapidity of the semiconductor chip 1 which exceeds 50MHz of frequencies of operation, and the appearance of the multilayer-interconnection substrate 3 of a semiconductor package is not enlarged. Moreover, since height 5a is prepared for the cap 5, positioning of the cap 5 to a substrate 3 becomes easy, and a position gap of a cap 5 can be prevented. Moreover, reliability of chip-capacitor 8b improves sharply, without separating by the external environment, since it is completely covered by the sealing resin 6. Furthermore, since the chip used as hindrance stopped existing on multilayer-interconnection substrate 3 front face like before also about a radiation fin 9, what has good thermal efficiency large-sized can be carried.
[0021] In addition, although invention which formed the chip capacitor in the interior of a substrate like JP,3-225859,B is proposed from the former, when based on such invention, the number of processes of a substrate will increase and a manufacturing cost will become high here. this invention aims at supplying the substrate which enables operation by the RF at cost of the same grade as the conventional substrate manufacturing cost to such a conventional example.
[0022] The perspective diagram and drawing 4 which show example 2., next a semiconductor device [in / the example 2 of this invention / in drawing 3] are the cross section. The wire which a semiconductor chip and 2 become from aluminum or gold in these drawings in 1, The multilayer-interconnection substrate which 3 becomes from FR4 or BT resin, the solder ball with which 4 consists of lead and tin, The cap which 5 becomes from BT resin or a ceramic, and 6 chip-capacitor 8b with a cap 5 A wrap sealing resin, The metal plate which consists of a cap resin with which 6a closes a cap, a metal with which 7 consists of copper or a copper alloy, The mass chip capacitor which 8b becomes from a ceramic, the radiation fin which 9 becomes from aluminum or copper, and 11 are the multilayer-interconnection substrate 3 and the spot facing by which the cap 5 was formed in the wrap sealing section and 11a by the sealing section 11 by the sealing resin 6. In this example, the aforementioned sealing section 11 is a portion which a cap's 5 flat surface does not counter. In this example, the land 10 set to spot facing 11a of this sealing section 11 from conductors, such as gold or copper, is formed by the leader of power supply layer 10a inside the multilayer-interconnection substrate 3, and grand layer 10b.
[0023] In an example 2, when closing a cap 5 in the sealing section 11, after attaching chip-capacitor 8b in a land 10 by the electroconductive glue (illustration ellipsis), chip-capacitor 8b of the cap 5 and plurality in the sealing resin 6 is covered.
[0024] According to this example, two or more spot facing 11a was prepared in the sealing section 11 as mentioned above, and mass chip-capacitor 8b is attached in the land 10 of this spot facing 11a. Therefore, the rapidity of the chip exceeding 50MHz of frequencies of operation can be secured like an example 1, and the appearance of the multilayer-interconnection substrate 3 of a semiconductor package is not enlarged. Moreover, since a cap's 5 configuration may be the same as that of the former, the manufacturing cost is the same as usual. Moreover, reliability of chip-capacitor 8b also improves, without separating from a substrate 3 by the external environment, since it is completely covered by the sealing resin 6.
[0025] In addition, although the land 10 for attaching the aforementioned chip-capacitor 8b is formed in spot facing 11a of the sealing section 11 and this spot facing 11a is formed in the example 2 as a crevice which followed the centrum in the centrum of a substrate 3 A crevice is established in the field by the side of the cap seal of a substrate 3 separately from a centrum, and you may make it form the land for attaching a chip in this crevice in the place besides for example, not the thing restricted to this but the aforementioned centrum in this invention.
[0026] The perspective diagram and drawing 6 which show the semiconductor device according [example 3., next drawing 5] to the example 3 of this invention are the cross section. The wire which a

semiconductor chip and 2 become from aluminum or gold in these drawings in 1, The multilayer-interconnection substrate which 3 becomes from FR4 or BT resin, the solder ball with which 4 consists of lead and tin, The cap which 5 becomes from BT resin or a ceramic, the cap resin with which 6a closes a cap 5, The metal plate with which 7 consists of copper or a copper alloy, the mass chip capacitor which 8b becomes from a ceramic, The radiation fin which 9 becomes from aluminum or copper, the land which 10 becomes from conductors, such as gold or copper The sealing section in which 11 closes the multilayer-interconnection substrate 3 and a cap 5, and 11b are the spot facing (crevice) formed in the lower layer side of the portion which counters the flat surface of the aforementioned cap 5 of the sealing section 11 of the multilayer-interconnection substrate 3. That is, as shown in drawing 7 , this spot facing 11b is formed in the sealing section 11 of a substrate 3 in the centrum of a substrate 3 as a crevice of the cap 5 loading section further prolonged in a lower layer.

[0027] In this example, the cap 5 has covered the whole field portion of chip-capacitor 8b. Two or more spot facing 11b prolonged to the lower layer side of the multilayer-interconnection substrate 3 was prepared in the sealing section 11 which attaches chip-capacitor 8b, and the land 10 which pulled out the conductor from the multilayer-interconnection substrate 3 interior is formed in this spot facing 11b. The land 10 is formed from the leader of power supply layer 10a inside the multilayer-interconnection substrate 3, and grand layer 10b.

[0028] When closing a cap 5 in the sealing section 11, after attaching chip-capacitor 8b in a land 10 by the electroconductive glue (illustration ellipsis), it is made to cover chip-capacitor 8b of the cap 5 and plurality in cap resin 6a in this example.

[0029] As mentioned above, two or more spot facing (crevice) 11b prolonged to the lower layer side of the multilayer-interconnection substrate 3 is prepared in the sealing section 11, and it is made to attach chip-capacitor 8b in this spot facing 11b in this example. Therefore, the rapidity of the chip exceeding 50MHz of frequencies of operation can be secured like an example 1, and the appearance of the multilayer-interconnection substrate 3 of a semiconductor package is not enlarged. Moreover, since a cap's 5 configuration may be the same as that of the former, it does not raise a manufacturing cost. Moreover, reliability of chip-capacitor 8b also comes to improve, without separating by the external environment, since it is completely covered by cap resin 6a.

[0030] The example 4 of this invention is explained based on example 4., next drawing 8 . This example 4 is a modification of the above-mentioned example 3. The same sign is given to the portion which is common in drawing 6 in drawing 8 . In this example 4, the cap 5 is closed with the sealing resin 6 on the field by the side of the cap seal of the multilayer-interconnection substrate 3. Moreover, in this example 4, crevice 11c which follows a centrum is formed in the flat surface of the aforementioned cap 5 in the centrum of a substrate 3, and the portion which counters, and the land (not shown) for attaching chip-capacitor 8b in this crevice 11c is formed. In this example 4, although the cap 5 is formed on the field of a substrate 3, only the part has thin-shape-ized the substrate 3. Therefore, the almost same effect as an example 3 can be done so also according to this example 4 -- thin shape-ization of the whole semiconductor device can be attained.

[0031]

[Effect of the Invention] With the semiconductor device by this invention, as explained above, since the chip is attached in the land formed in the portion which counters the flat surface of the notch of the aforementioned cap of the centrum of the aforementioned substrate, a cap ceases to cover a chip top and the whole semiconductor device comes to be thin-shape-ized. Moreover, since a chip is attached in the cap-seal side of a substrate and does not interfere with the radiation fin by the side of the front face of a substrate, it is lost that the size of a radiation fin is restricted of it by the chip like before. Furthermore, since a chip is attached in a position so that it may lap with the aforementioned cap in the direction of a flat surface of a substrate, by the external environment, most possibility of separating from a substrate disappears and its reliability comes to improve.

[0032] Moreover, in the semiconductor device by this invention, since it is made to attach a chip in the crevice formed in the portion which does not counter the flat surface of the aforementioned cap of the aforementioned substrate, to a chip, a cap flat surface ceases to counter and the whole semiconductor

device comes to be thin-shape-ized. Moreover, since a chip is attached in the cap-seal side of a substrate and does not interfere with the radiation fin by the side of the front face of a substrate, it is lost that the size of a radiation fin is restricted of it by the chip like before. Furthermore, since a chip is attached in a position so that it may lap with the aforementioned cap in the direction of a flat surface of a substrate, by the external environment, most possibility of separating from a substrate disappears and its reliability comes to improve.

[0033] Moreover, in the semiconductor device by this invention, it can prevent now completely that a chip separates from the chip in which the above was attached from a substrate by the external environment by closing with the sealing resin around the aforementioned cap and a cap, and reliability comes to improve it sharply.

[0034] Moreover, in the semiconductor device by this invention, since it is made to attach a chip in the crevice formed in the portion which counters the flat surface of the aforementioned cap in the centrum of the aforementioned substrate, it does not become the relation in which a chip interferes mutually with a cap in the direction of a flat surface of a substrate, but the whole semiconductor device comes to be thin-shape-ized. Moreover, since a chip is attached in the cap-seal side of a substrate and does not interfere with the radiation fin by the side of the front face of a substrate, it is lost that the size of a radiation fin is restricted of it by the chip like before. Furthermore, since a chip is attached in a position so that it may lap with the aforementioned cap in the direction of a flat surface of a substrate, by the external environment, most possibility of separating from a substrate disappears and its reliability comes to improve.

[0035] Furthermore, in the semiconductor device by this invention, since it is made to attach a chip capacitor as the aforementioned chip, even when attaching the capacitor for noise rejection, in order to attach on the surface of a substrate like before, it is lost that the thickness of the whole semiconductor device becomes large. Moreover, it becomes, without the size of a radiation fin being restricted by the capacitor attached in the substrate front face like before. Furthermore, it is prevented that the capacitor attached in the substrate front face separates by the external environment etc., and its reliability comes to improve.

[Translation done.]

* NOTICES *

1. This document has been translated by computer.So the translation may not reflect the original precisely.
2. **** shows the word which can not be translated.
3.In the drawings, any words are not translated.

TECHNICAL FIELD

[Industrial Application] This invention relates to the semiconductor device which has the hollow type semiconductor package which carries out the cap seal of the semiconductor chip to the centrum of a multilayer-interconnection substrate.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

PRIOR ART

[Description of the Prior Art] The perspective diagram and drawing 10 which show the semiconductor package of the former [drawing 9] are the cross section. The wire which a semiconductor chip and 2 become from aluminum or gold in these drawings in 1, The multilayer-interconnection substrate which 3 becomes from FR4 or BT resin, the solder ball with which 4 consists of lead and tin, The cap which 5 becomes from BT resin or a ceramic, the sealing resin with which 6 closes a cap 5, The metal plate with which 7 consists of copper or a copper alloy, the small capacity chip capacitor which 8a becomes from a ceramic, the mass chip capacitor which 8b becomes from a ceramic, and 9 are radiation fins which consist of aluminum or copper.
[0003] Thus, in the conventional hollow type semiconductor package, two or more solder balls 4 are arranged on the front face on the multilayer-interconnection substrate 3, and the wire 2 which connects a semiconductor chip 1 and a semiconductor chip 1, and the multilayer-interconnection substrate 3 to the centrum of multilayer-interconnection substrate 3 center is contained, and the seal of these semiconductor chips 1, wires 2, etc. is further done by the cap 5. On the other hand, the metal plate 7 which consists of copper or a copper alloy for radiating the heat from a semiconductor chip 1 etc. is formed in the center of a front face of the multilayer-interconnection substrate 3, and the radiation fin 9 which consists of aluminum or copper is further attached on this metal plate 7.

[Translation done.]

* NOTICES *

1. This document has been translated by computer.So the translation may not reflect the original precisely.
2. **** shows the word which can not be translated.
3.In the drawings, any words are not translated.

EFFECT OF THE INVENTION

[Effect of the Invention] With the semiconductor device by this invention, as explained above, since the chip is attached in the land formed in the portion which counters the flat surface of the notch of the aforementioned cap of the centrum of the aforementioned substrate, a cap ceases to cover a chip top and the whole semiconductor device comes to be thin-shape-ized. Moreover, since a chip is attached in the cap-seal side of a substrate and does not interfere with the radiation fin by the side of the front face of a substrate, it is lost that the size of a radiation fin is restricted of it by the chip like before. Furthermore, since a chip is attached in a position so that it may lap with the aforementioned cap in the direction of a flat surface of a substrate, by the external environment, most possibility of separating from a substrate disappears and its reliability comes to improve.

[0032] Moreover, in the semiconductor device by this invention, since it is made to attach a chip in the crevice formed in the portion which does not counter the flat surface of the aforementioned cap of the aforementioned substrate, to a chip, a cap flat surface ceases to counter and the whole semiconductor device comes to be thin-shape-ized. Moreover, since a chip is attached in the cap-seal side of a substrate and does not interfere with the radiation fin by the side of the front face of a substrate, it is lost that the size of a radiation fin is restricted of it by the chip like before. Furthermore, since a chip is attached in a position so that it may lap with the aforementioned cap in the direction of a flat surface of a substrate, by the external environment, most possibility of separating from a substrate disappears and its reliability comes to improve.

[0033] Moreover, in the semiconductor device by this invention, it can prevent now completely that a chip separates from the chip in which the above was attached from a substrate by the external environment by closing with the sealing resin around the aforementioned cap and a cap, and reliability comes to improve it sharply.

[0034] Moreover, in the semiconductor device by this invention, since it is made to attach a chip in the crevice formed in the portion which counters the flat surface of the aforementioned cap in the centrum of the aforementioned substrate, it does not become the relation in which a chip interferes mutually with a cap in the direction of a flat surface of a substrate, but the whole semiconductor device comes to be thin-shape-ized. Moreover, since a chip is attached in the cap-seal side of a substrate and does not interfere with the radiation fin by the side of the front face of a substrate, it is lost that the size of a radiation fin is restricted of it by the chip like before. Furthermore, since a chip is attached in a position so that it may lap with the aforementioned cap in the direction of a flat surface of a substrate, by the external environment, most possibility of separating from a substrate disappears and its reliability comes to improve.

[0035] Furthermore, in the semiconductor device by this invention, since it is made to attach a chip capacitor as the aforementioned chip, even when attaching the capacitor for noise rejection, in order to attach on the surface of a substrate like before, it is lost that the thickness of the whole semiconductor device becomes large. Moreover, it becomes, without the size of a radiation fin being restricted by the capacitor attached in the substrate front face like before. Furthermore, it is prevented that the capacitor attached in the substrate front face separates by the external environment etc., and its reliability comes to

improve.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] By the way, the above chip capacitors 8a and 8b are required in order to achieve an operation of the noise rejection for securing the rapidity of the semiconductor chip exceeding 50MHz etc. And in the conventional semiconductor device, as such chip capacitors 8a and 8b are shown in drawing 10 , mounting in the front face of the aforementioned multilayer-interconnection substrate 3 is performed.
[0005] However, as shown, for example in drawing 10 , when small capacity chip-capacitor 8a is mounted in the front face of the multilayer-interconnection substrate 3, it is necessary to attach a radiation fin 9 on chip-capacitor 8a, and there is a problem that the thickness of the whole semiconductor device will become large. Moreover, as shown in drawing 10 , when mass chip-capacitor 8b is mounted in the front face of the multilayer-interconnection substrate 3, this mass chip-capacitor 8b must be avoided, it is necessary to attach a radiation fin 9, size of a radiation fin 9 must be made so small, and there is a problem that efficient and sufficient discharge of the heat from a semiconductor chip 1 cannot be performed. Furthermore, as shown in drawing 10 , when mass chip-capacitor 8b etc. is mounted in the front face of the multilayer-interconnection substrate 3, there is a problem that a chip capacitor will separate from a substrate 3 by the external environment.
[0006] this invention was made paying attention to the trouble of such conventional technology, even if it mounts chips, such as a chip capacitor, it can maintain the whole semiconductor device at a thin shape, even if it mounts chips, such as a chip capacitor, a radiation fin can use the thing of big size, and it aims at offering a semiconductor device without a possibility that chips, such as a chip capacitor, may separate from a substrate further.

[Translation done.]

* NOTICES *

1. This document has been translated by computer.So the translation may not reflect the original precisely.
2. **** shows the word which can not be translated.
3.In the drawings, any words are not translated.

MEANS

[Means for Solving the Problem] In the semiconductor device by this invention for solving such a technical problem, a semiconductor chip is carried in the centrum of a substrate, a notch is formed in some aforementioned caps in the semiconductor device with which the cap seal of this semiconductor chip is carried out, and it changes, and the land for chip installation is formed in the portion which counters the flat surface of the notch of the aforementioned cap of the centrum of the aforementioned substrate.
[0008] Moreover, in the semiconductor device by this invention, a semiconductor chip is carried in the centrum of a substrate and the crevice for chip installation is formed in the portion to which this semiconductor chip does not counter the flat surface of the aforementioned cap of the aforementioned substrate in the semiconductor device which a cap seal is carried out and changes.
[0009] Moreover, as for the chip in which the above was attached in the semiconductor device by this invention, it is desirable to be closed with the sealing resin around the aforementioned cap and a cap.
[0010] Moreover, in the semiconductor device by this invention, a semiconductor chip is carried in the centrum of a substrate and the crevice for chip installation is formed in the portion to which this semiconductor chip counters the flat surface of the aforementioned cap in the centrum of the aforementioned substrate in the semiconductor device which a cap seal is carried out and changes.
[0011] As for the aforementioned chip, in the semiconductor device by this invention, it is still more desirable that it is a chip capacitor.

[Translation done.]

* NOTICES *

1. This document has been translated by computer.So the translation may not reflect the original precisely.
2. **** shows the word which can not be translated.
3.In the drawings, any words are not translated.

OPERATION

[Function] As mentioned above, in the semiconductor device by this invention, a notch is formed in some aforementioned caps and the land for chip installation is formed in the portion which counters the flat surface of the notch of the aforementioned cap of the centrum of the aforementioned substrate. Therefore, in this invention, when a chip is attached in the aforementioned land, a cap's notch counters on this chip and a cap covers a chip top. That is, in this invention, a chip and a cap are stationed so that it may lap mutually in the direction of a flat surface of a substrate, and so that it may not lap mutually in the thickness direction of a substrate. Therefore, the whole semiconductor device comes to be thin-shape-ized. Moreover, in this invention, since a chip is attached in the cap-seal side of a substrate and does not interfere with the radiation fin by the side of the front face of a substrate, it is lost that the size of a radiation fin is restricted of it by the chip like before. Furthermore, by this invention, since a chip is attached in a position so that it may lap with the aforementioned cap in the direction of a flat surface of a substrate, most possibility of separating from a substrate by the external environment disappears.
[0013] Moreover, the crevice for chip installation is formed in the portion which does not counter the flat surface of the aforementioned cap of the aforementioned substrate in the semiconductor device by this invention. Therefore, in this invention, when a chip is attached in the aforementioned crevice, a cap flat surface does not counter to this chip. That is, in this invention, a chip and a cap are stationed so that it may lap mutually in the direction of a flat surface of a substrate, and so that it may not lap mutually about the thickness direction of a substrate. Therefore, the whole semiconductor device comes to be thin-shape-ized. Moreover, in this invention, since a chip is attached in the cap-seal side of a substrate and does not interfere with the radiation fin by the side of the front face of a substrate, it is lost that the size of a radiation fin is restricted of it by the chip like before. Furthermore, by this invention, since a chip is attached in a position so that it may lap with the aforementioned cap in the direction of a flat surface of a substrate, most possibility of separating from a substrate by the external environment disappears. In addition, in this invention, the crevice for the aforementioned chip installation may be prepared in the centrum of a substrate, and may be prepared out of the centrum of a substrate.
[0014] Moreover, in the semiconductor device by this invention, it can prevent now completely that a chip separates from the chip in which the above was attached from a substrate by the external environment by closing with the sealing resin around the aforementioned cap and a cap.
[0015] Moreover, the crevice for chip installation is formed in the portion which counters the flat surface of the aforementioned cap of the centrum of the aforementioned substrate in the semiconductor device by this invention. Therefore, in this invention, when a chip is attached in the aforementioned crevice, although this chip becomes the relation which overlap mutually in the thickness direction of a substrate to a cap, since it is attached in the crevice formed in the centrum, it does not become the relation in which it interferes mutually with a cap in the direction of a flat surface of a substrate. Therefore, the whole semiconductor device comes to be thin-shape-ized. Moreover, in this invention, since a chip is attached in the cap-seal side of a substrate and does not interfere with the radiation fin by the side of the front face of a substrate, it is lost that the size of a radiation fin is restricted of it by the chip like before. Furthermore, by this invention, since a chip is attached in a position so that it may lap

with the aforementioned cap in the direction of a flat surface of a substrate, most possibility of separating from a substrate by the external environment disappears.
[0016] It is made to attach a chip capacitor as the aforementioned chip in the semiconductor device by this invention furthermore. Therefore, even when attaching the capacitor for noise rejection, in order to attach on the surface of a substrate like before, it is lost that the thickness of the whole semiconductor device becomes large. Moreover, it becomes, without the size of a radiation fin being restricted by the capacitor attached in the substrate front face like before. Furthermore, it comes to be prevented that the capacitor attached in the substrate front face separates by the external environment etc.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

EXAMPLE

[Example]
The perspective diagram and drawing 2 which show a semiconductor device [in / the example 1 of this invention / in example 1. drawing 1] are the cross section of the semiconductor device of this example 1. The wire which a semiconductor chip and 2 become from aluminum or gold in these drawings in 1, The multilayer-interconnection substrate which 3 becomes from FR4 or BT resin, the solder ball with which 4 consists of lead and tin, The cap and 5a which 5 becomes from BT resin or a ceramic A cap's height, The cap resin with which, as for a wrap sealing resin and 6a, a cap 5 and a chip capacitor are applied to 6 by a cap's 5 inferior surface of tongue, the metal plate with which 7 consists of copper or a copper alloy, the mass chip capacitor which 8b becomes from a ceramic, and 9 are radiation fins which consist of aluminum or copper. Moreover, in drawing, 10 is the land which consists of conductors, such as gold or copper, and consists of power supply layer 10a inside the multilayer-interconnection substrate 3, and an outgoing line of grand layer 10b. Moreover, in drawing, 11 is the wrap sealing section by the sealing resin 6 about the multilayer-interconnection substrate 3 and a cap 5.
[0018] In addition, in this example, a portion without the aforementioned height 5a in the aforementioned cap's 5 periphery section is equivalent to the "notch" portion of the cap 5 who says this invention. Moreover, the sealing section 11 put into the aforementioned sealing resin 6 has countered this cap's 5 "notch" portion in the thickness direction of a substrate 3. That is, in this example, the aforementioned cap 5 is formed so that there may be no portion of the cap 5 who counters in the substrate thickness direction to the field portion of chip-capacitor 8b, and the portion may serve as a "notch." moreover, the portion which does not counter in the substrate thickness direction to the field portion of a cap's 5 aforementioned chip-capacitor 8b -- above -- a notch -- him -- height 5a is formed in the meaning that there is no **** This height 5a is used in order to position a cap 5 with high precision to the centrum of a substrate 3 when attaching a cap 5, and contacted by the wall side of the centrum of a substrate 3.
[0019] Moreover, in this example, the land 10 which pulled out the conductor from the multilayer-interconnection substrate 3 interior is formed in the sealing section 11 which attaches chip-capacitor 8b. When closing a cap 5 in the sealing section 11, after attaching chip-capacitor 8b in a land 10 by the electroconductive glue (illustration ellipsis), a cap 5 is closed by the cap resin 6, and it is made to cover chip-capacitor 8b by the sealing resin 6 after that. In addition, although a cap 5 is closed by the sealing resin 6, a cap 5 is closed by the cap resin 6 before a wrap and it is made to cover chip-capacitor 8b by the sealing resin 6 after that in this example 1, without using the cap resin 6, chip-capacitor 8b is attached in a land 10 by the electroconductive glue (illustration ellipsis), and it is good [in a cap 5 and the aforementioned chip-capacitor 8b] by the sealing resin 6 as for a method of a wrap after that.
[0020] As mentioned above, according to this example, since two or more mass chip-capacitor 8b is prepared in the cap 5 side of a substrate 3, for example, it can fully secure also by the rapidity of the semiconductor chip 1 which exceeds 50MHz of frequencies of operation, and the appearance of the multilayer-interconnection substrate 3 of a semiconductor package is not enlarged. Moreover, since height 5a is prepared for the cap 5, positioning of the cap 5 to a substrate 3 becomes easy, and a position

gap of a cap 5 can be prevented. Moreover, reliability of chip-capacitor 8b improves sharply, without separating by the external environment, since it is completely covered by the sealing resin 6. Furthermore, since the chip used as hindrance stopped existing on multilayer-interconnection substrate 3 front face like before also about a radiation fin 9, what has good thermal efficiency large-sized can be carried.

[0021] In addition, although invention which formed the chip capacitor in the interior of a substrate like JP,3-225859,B is proposed from the former, when based on such invention, the number of processes of a substrate will increase and a manufacturing cost will become high here. this invention aims at supplying the substrate which enables operation by the RF at cost of the same grade as the conventional substrate manufacturing cost to such a conventional example.

[0022] The perspective diagram and drawing 4 which show example 2., next a semiconductor device [in / the example 2 of this invention / in drawing 3] are the cross section. The wire which a semiconductor chip and 2 become from aluminum or gold in these drawings in 1, The multilayer-interconnection substrate which 3 becomes from FR4 or BT resin, the solder ball with which 4 consists of lead and tin, The cap which 5 becomes from BT resin or a ceramic, and 6 chip-capacitor 8b with a cap 5 A wrap sealing resin, The metal plate which consists of a cap resin with which 6a closes a cap, a metal with which 7 consists of copper or a copper alloy, The mass chip capacitor which 8b becomes from a ceramic, the radiation fin which 9 becomes from aluminum or copper, and 11 are the multilayer-interconnection substrate 3 and the spot facing by which the cap 5 was formed in the wrap sealing section and 11a by the sealing section 11 by the sealing resin 6. In this example, the aforementioned sealing section 11 is a portion which a cap's 5 flat surface does not counter. In this example, the land 10 set to spot facing 11a of this sealing section 11 from conductors, such as gold or copper, is formed by the leader of power supply layer 10a inside the multilayer-interconnection substrate 3, and grand layer 10b.

[0023] In an example 2, when closing a cap 5 in the sealing section 11, after attaching chip-capacitor 8b in a land 10 by the electroconductive glue (illustration ellipsis), chip-capacitor 8b of the cap 5 and plurality in the sealing resin 6 is covered.

[0024] According to this example, two or more spot facing 11a was prepared in the sealing section 11 as mentioned above, and mass chip-capacitor 8b is attached in the land 10 of this spot facing 11a. Therefore, the rapidity of the chip exceeding 50MHz of frequencies of operation can be secured like an example 1, and the appearance of the multilayer-interconnection substrate 3 of a semiconductor package is not enlarged. Moreover, since a cap's 5 configuration may be the same as that of the former, the manufacturing cost is the same as usual. Moreover, reliability of chip-capacitor 8b also improves, without separating from a substrate 3 by the external environment, since it is completely covered by the sealing resin 6.

[0025] In addition, although the land 10 for attaching the aforementioned chip-capacitor 8b is formed in spot facing 11a of the sealing section 11 and this spot facing 11a is formed in the example 2 as a crevice which followed the centrum in the centrum of a substrate 3 A crevice is established in the field by the side of the cap seal of a substrate 3 separately from a centrum, and you may make it form the land for attaching a chip in this crevice in the place besides for example, not the thing restricted to this but the aforementioned centrum in this invention.

[0026] The perspective diagram and drawing 6 which show the semiconductor device according [example 3., next drawing 5] to the example 3 of this invention are the cross section. The wire which a semiconductor chip and 2 become from aluminum or gold in these drawings in 1, The multilayer-interconnection substrate which 3 becomes from FR4 or BT resin, the solder ball with which 4 consists of lead and tin, The cap which 5 becomes from BT resin or a ceramic, the cap resin with which 6a closes a cap 5, The metal plate with which 7 consists of copper or a copper alloy, the mass chip capacitor which 8b becomes from a ceramic, The radiation fin which 9 becomes from aluminum or copper, the land which 10 becomes from conductors, such as gold or copper The sealing section in which 11 closes the multilayer-interconnection substrate 3 and a cap 5, and 11b are the spot facing (crevice) formed in the lower layer side of the portion which counters the flat surface of the aforementioned cap 5 of the

sealing section 11 of the multilayer-interconnection substrate 3. That is, as shown in drawing 7 , this spot facing 11b is formed in the sealing section 11 of a substrate 3 in the centrum of a substrate 3 as a crevice of the cap 5 loading section further prolonged in a lower layer.

[0027] In this example, the cap 5 has covered the whole field portion of chip-capacitor 8b. Two or more spot facing 11b prolonged to the lower layer side of the multilayer-interconnection substrate 3 was prepared in the sealing section 11 which attaches chip-capacitor 8b, and the land 10 which pulled out the conductor from the multilayer-interconnection substrate 3 interior is formed in this spot facing 11b. The land 10 is formed from the leader of power supply layer 10a inside the multilayer-interconnection substrate 3, and grand layer 10b.

[0028] When closing a cap 5 in the sealing section 11, after attaching chip-capacitor 8b in a land 10 by the electroconductive glue (illustration ellipsis), it is made to cover chip-capacitor 8b of the cap 5 and plurality in cap resin 6a in this example.

[0029] As mentioned above, two or more spot facing (crevice) 11b prolonged to the lower layer side of the multilayer-interconnection substrate 3 is prepared in the sealing section 11, and it is made to attach chip-capacitor 8b in this spot facing 11b in this example. Therefore, the rapidity of the chip exceeding 50MHz of frequencies of operation can be secured like an example 1, and the appearance of the multilayer-interconnection substrate 3 of a semiconductor package is not enlarged. Moreover, since a cap's 5 configuration may be the same as that of the former, it does not raise a manufacturing cost. Moreover, reliability of chip-capacitor 8b also comes to improve, without separating by the external environment, since it is completely covered by cap resin 6a.

[0030] The example 4 of this invention is explained based on example 4., next drawing 8 . This example 4 is a modification of the above-mentioned example 3. The same sign is given to the portion which is common in drawing 6 in drawing 8 . In this example 4, the cap 5 is closed with the sealing resin 6 on the field by the side of the cap seal of the multilayer-interconnection substrate 3. Moreover, in this example 4, crevice 11c which follows a centrum is formed in the flat surface of the aforementioned cap 5 in the centrum of a substrate 3, and the portion which counters, and the land (not shown) for attaching chip-capacitor 8b in this crevice 11c is formed. In this example 4, although the cap 5 is formed on the field of a substrate 3, only the part has thin-shape-ized the substrate 3. Therefore, the almost same effect as an example 3 can be done so also according to this example 4 -- thin shape-ization of the whole semiconductor device can be attained.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the perspective diagram showing the semiconductor device by the example 1 of this invention.
[Drawing 2] It is the cross section showing the semiconductor device by the example 1 of this invention.

[Drawing 3] It is the perspective diagram showing the semiconductor device by the example 2 of this invention.
[Drawing 4] It is the cross section showing the semiconductor device by the example 2 of this invention.

[Drawing 5] It is the perspective diagram showing the semiconductor device by the example 3 of this invention.
[Drawing 6] It is the cross section showing the semiconductor device by the example 3 of this invention.

[Drawing 7] It is the shown perspective diagram for explaining the spot facing of the example 3 of this invention.
[Drawing 8] It is the cross section showing the semiconductor device by the example 4 of this invention.

[Drawing 9] It is the perspective diagram showing the conventional semiconductor device.
[Drawing 10] It is the cross section showing the conventional semiconductor device.
[Description of Notations]
1 Semiconductor Chip . Metal Plate . 8B Chip-Capacitor .9 Radiation-Fin . 10 Land . 10a Power Supply Layer .10B Grand Layer . 11 Sealing Section . 11a, 11B Spot Facing .11C Crevice 2 Wire . 3 Multilayer-Interconnection Substrate .4 Solder Ball . 5 Cap . 5a Height .6 Sealing Resin . 7

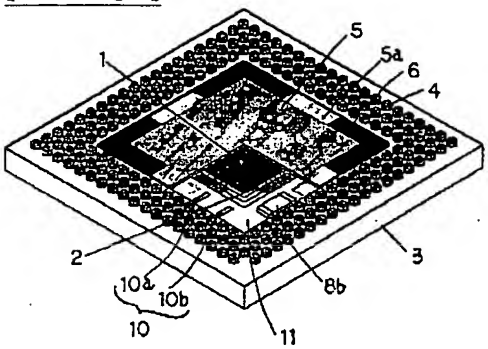
[Translation done.]

* NOTICES *

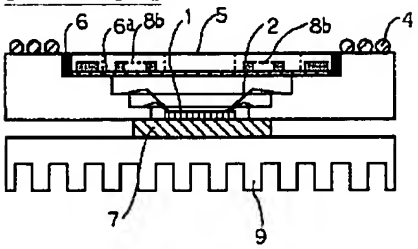
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

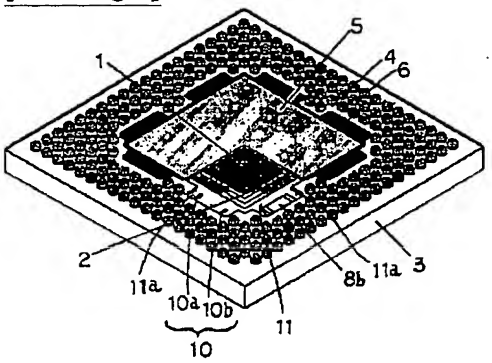
[Drawing 1]



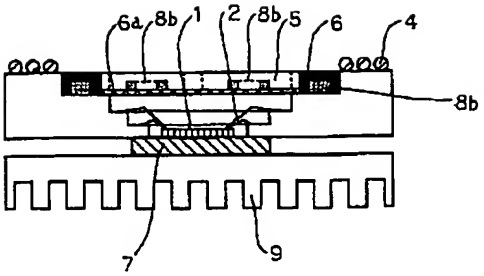
[Drawing 2]



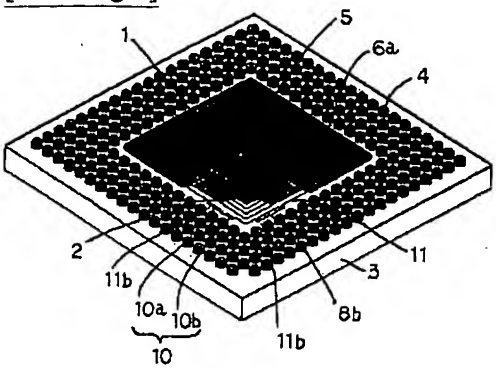
[Drawing 3]



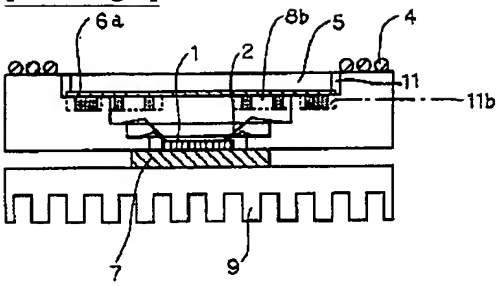
[Drawing 4]



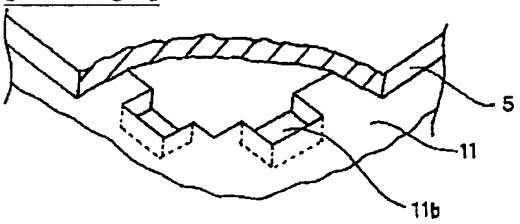
[Drawing 5]



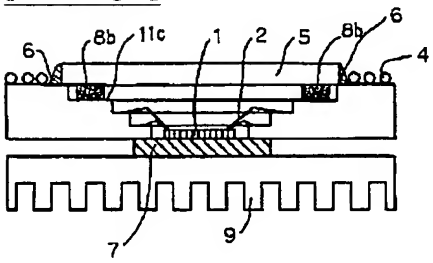
[Drawing 6]



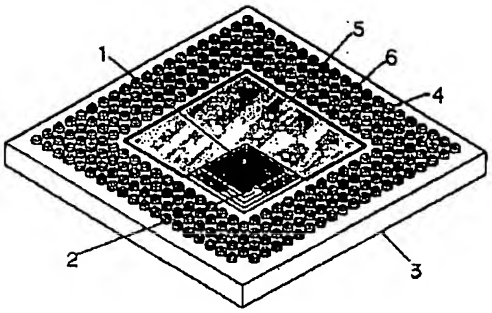
[Drawing 7]



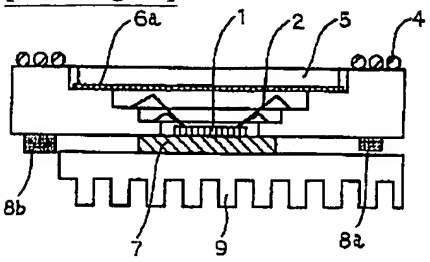
[Drawing 8]



[Drawing 9]



[Drawing 10]



[Translation done.]

Query/Command : his

File : PLUSPAT

SS	Results	
1	3	(1) ..FAM JP2001052498/PN
2	0	..FAM JP2000379569/PN
3	0	..FAM JP2000379567/PN
4	1	..CITB JP2001052498/PN
5	1	..CITF JP2001052498/PN
6	0	..CITB JP2000379569/PN

Search statement 7

1 / 3 *PLUSPAT - ©QUESTEL-ORBIT*

PN - TW451458 B 20010821 [TW-451458]
TI - (B) Semiconductor memory device
PA - (B) TOKYO SHIBAURA ELECTRIC CO (JP)
IN - (B) NAKAMURA KENICHI (JP)
AP - TW89115712 20000804 [2000TW-0115712]
PR - JP22278199 19990805 [1999JP-0222781]
IC - (B) H01L-027/00
STG - (B) Patent
AB - The present invention provides a kind of clock synchronous semiconductor memory device capable of easily certifying and estimating its characteristics. For this device, a control signal generating circuit generates a word line pulse signal WLP, a writing pulse signal WP and a sense amplifier pulse signal SAP according to a clock signal CLK. In the SRAM for performing the control of reading/writing data of a memory cell array, a monitor control signal (PM) input terminal 14, output buffers 12a to 12c used for monitor and monitor output terminals 13a to 13c are provided such that the internal control signals can be monitored.+DBPH+ In addition, a switching control signal (PCS) input terminal 16, a writing pulse control signal (WPC) input terminal 18 and a sense amplifier pulse control signal (SAPC) input terminal 20 are installed such that it is capable of controlling the writing pulse signal WP and the sense amplifier pulse signal SAP from the outside. The word line pulse signal WLP can be controlled by the input of clock signal CLK from the clock signal input terminal 22.
UP - 2002-12

2 / 3 *PLUSPAT - ©QUESTEL-ORBIT - image*

PN - US6252820 B1 20010626 [US6252820]
TI - (B1) Semiconductor memory device capable of monitoring and adjusting the timing and pulse width of internal control signals
PA - (B1) TOKYO SHIBAURA ELECTRIC CO (US)
PA0 - Kabushiki Kaisha Toshiba, Kawasaki [JP]
IN - (B1) NAKAMURA KENICHI (JP)
AP - US63327700 20000804 [2000US-0633277]
PR - JP22278199 19990805 [1999JP-0222781]
IC - (B1) G11C-008/18
EC - G11C-007/22
G11C-011/418
PCL - ORIGINAL (O) : 365233000; CROSS-REFERENCE (X) : 365189030 365195000 365196000 365201000
DT - Basic
CT - US5208771; US5384735; US5384750; JP11-213660
STG - (B1) U.S. Patent (no pre-grant pub.) after Jan. 2, 2001
AB - A clock synchronous semiconductor memory device capable of easily certifying and estimating its characteristics comprises an SRAM for generating a word line pulse signal WLP, a writing pulse signal WP and a sense amplifier pulse signal SAP on the basis of a clock signal CLK from a control signal generating circuit 11, to control the reading/writing of data of a memory cell array. This SRAM comprises a monitor control signal (PM) input terminal 14, monitoring output buffers 12a through 12c and monitor output terminals 13a through 13c, so as to allow the monitoring of internal control signals. The SRAM further comprises a switching control signal (PCS) input terminal 16, a writing pulse control signal (WPC) input terminal 18 and a sense amplifier pulse control signal (SAPC) input terminal 20, so as to allow the control of the writing pulse signal WP and the sense amplifier pulse signal SAP from the outside. The word line pulse signal WLP can be

controlled by the input of the clock signal CLK from the clock signal input terminal 22.

UP - 2001-27

3 / 3 *PLUSPAT - ©QUESTEL-ORBIT - image*

PN - JP2001052498 A 20010223 [JP2001052498]

TI - SEMICONDUCTOR MEMORY

PA - (A) TOKYO SHIBAURA ELECTRIC CO

PA0 - (A) TOSHIBA CORP

IN - (A) NAKAMURA KENICHI

AP - JP22278199 19990805 [1999JP-0222781]

PR - JP22278199 19990805 [1999JP-0222781]

IC - (A) G11C-011/413 G11C-029/00

STG - (A) Doc. Laid open to publ. Inspec.

AB - PROBLEM TO BE SOLVED: To provide a clock synchronizing type semiconductor memory of which characteristics can be easily verified and evaluated.

SOLUTION: In a SRAM in which a word line pulse signal WLP, a write pulse signal WP, and a sense amplifier pulse signal SAP are generated by a control signal generating circuit 11 based on a clock signal CLK and read/ write control of data of a memory cell array is performed, the device is provided with a monitor control signal PM input terminal 14, output buffers 12a-12c for monitor, and monitor output terminals 13a-13c, and an internal control signal can be monitored. Further, the device is provided with a switching control signal PCS input terminal 16, a write pulse control signal WPC input terminal 18, and a sense amplifier pulse control signal SAPC input terminal 20, and the write pulse signal WP and the sense amplifier pulse signal SAP can be externally controlled. A word line pulse signal WLP can be controlled by an input of a clock signal CLK from a clock signal input terminal 22.

UP - 2001-12